KEYASIC
"SOC MADE SIMPLE"

www.keyasic.com

Key ASIC Corporate Profile

1. Founded in 2005

2. Public company - Listed in 2008 on Mainboard Bursa Malaysia

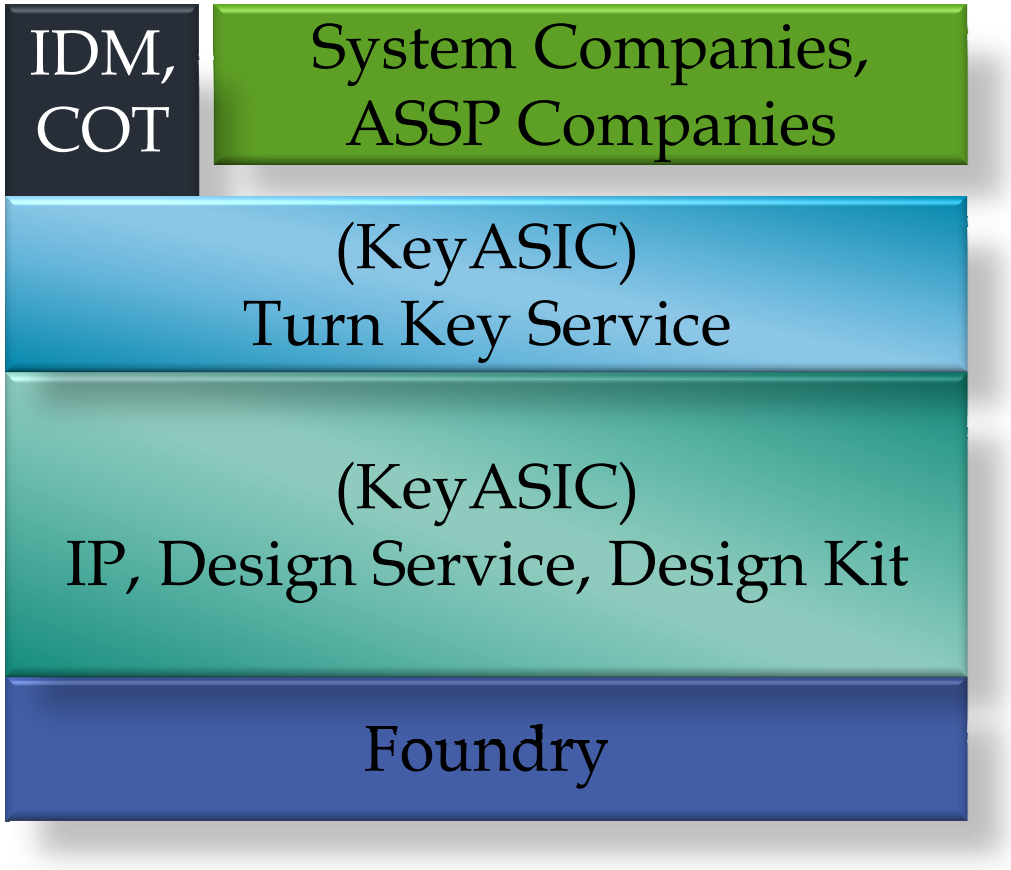
3. Capital: Share capital = RM$80,500,000 up to Nov., 2014

4. Offices:
   - R&D: Malaysia, Taiwan
   - Sales: Taiwan, Singapore

5. Core Business:
   - Turn-key ASIC design and production outsourcing, OEM and ODM
   - Customer Specific System Product (CSSP). Customer spec. into chip

6. Acquired Gateway Silicon – Taiwan, October 2009

KeyASIC's Roles



Significant Milestones

2005	Key ASIC Founded
2006	Profitable in for period ending 31 Dec 2006. Tape out over 10 SoC's on Silterra 0.18u, 0.16u, 0.13u.
1/2008	Shares traded on Mesdaq Market, Bursa Malaysia
9/2008	Engaged with IBM Microelectronics for 90nm, 65nm and 45nm technologies.
3/2009	Tape out 1st 65nm SoC on IBM.
4/2009	Started trading on Mainboard, Bursa Malaysia.
8/2009	Acquired GSI in Taiwan, a subsidiary of Macronix (invested by Chartered Semiconductor)
1/2010	Organization integration completed
2/2010	ISO9001:2008 Certified

Significant Milestones

2011	SMIC 0.18um eFlash capacitive touch ASIC project engagement
2011	TSMC 28nm FPGA APR project engagement
2012	Fujitsu 65nm ARM1176 HDTV project engagement
2012	Commercially shipment of 1st ASSP SOC for WiFi storage products
2013	MXIC 0.16um game ASIC MP, shipped over 3M pcs. chips
2013	Silterra 130nm 200MHz high performance DSP ASIC project engagement
2013	Silterra 0.13um ARM Cortex M3 MCU project engagement
2013	TSMC 0.18um SiGe RF chip project engagement
2014	GlobalFoundries 65nm ultra high speed DSP ASIC project engagement
2014	Fujitsu 65nm ARM1176 Baseband Processor project engagement
2014	Panasonic 65nm USB2 device PHY IP porting project engagement

Key ASIC – Well Positioned for Growth

- **3rd public listed company in the world, after GUC and Faraday in Taiwan**

- **Fastest growing company among the three**

Customers(1)

KeyASIC makes SoC/ASIC Design SIMPLE, BETTER!

Customers(2)

Transcend®

Lenovo

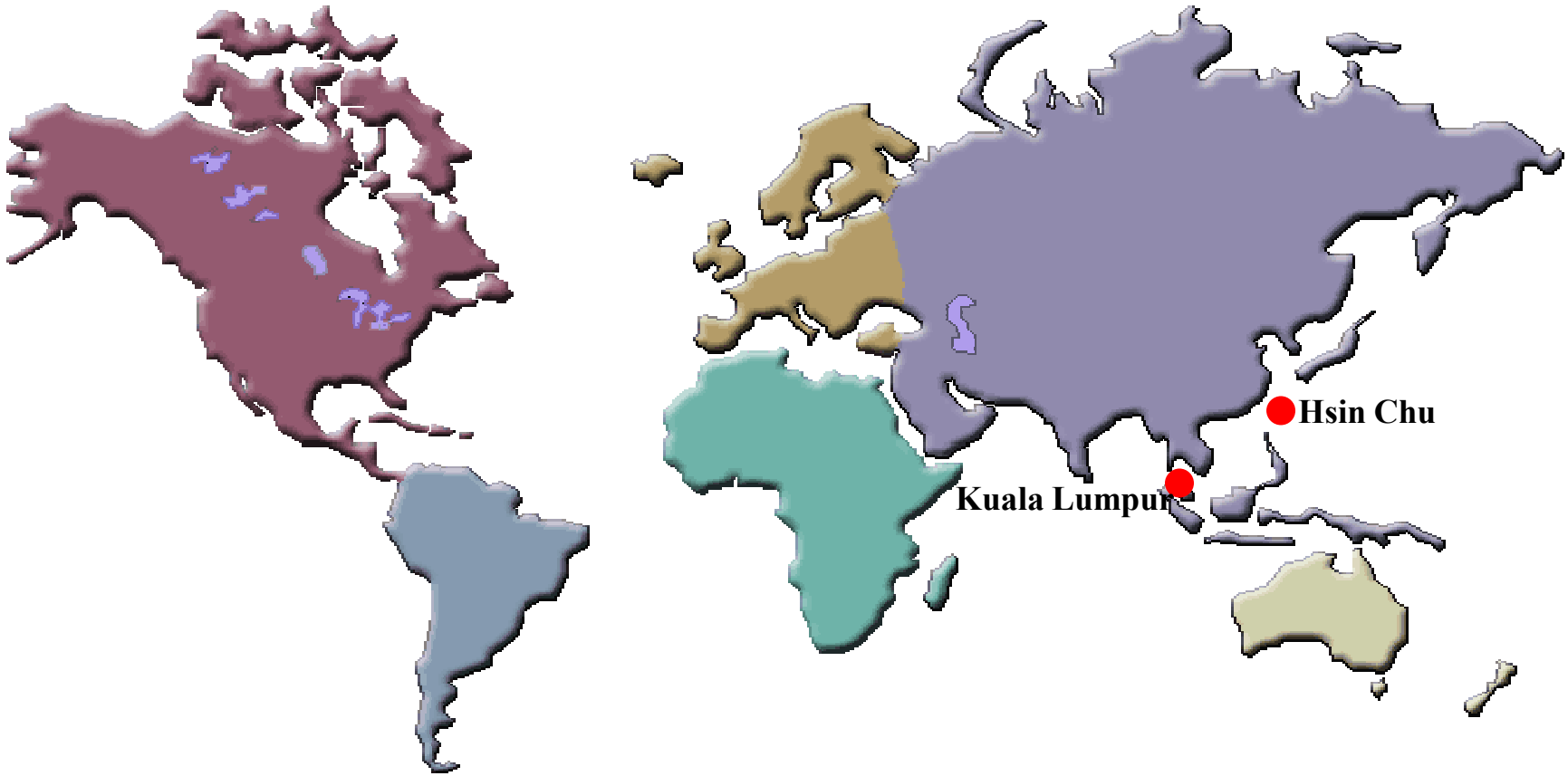
TOSHIBA
Leading Innovation

pqi

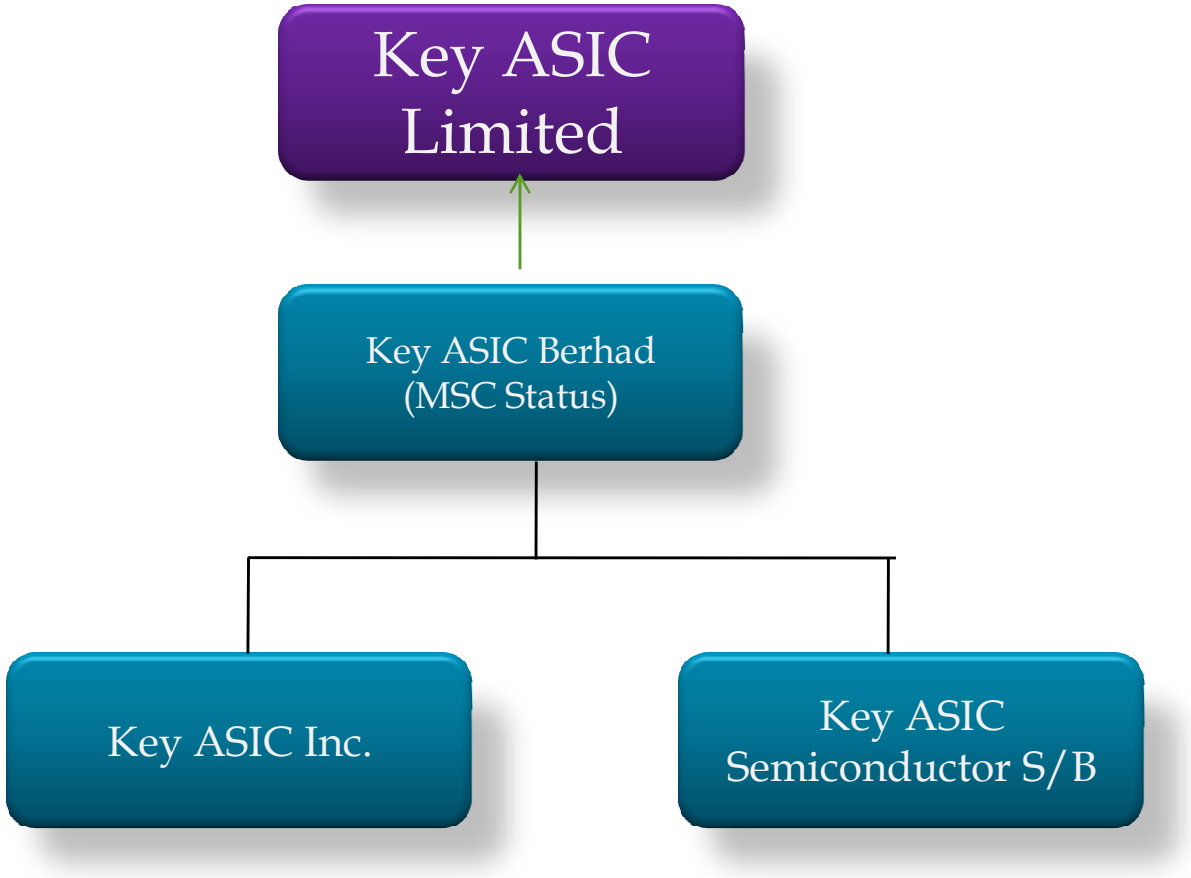
TREK

UPRtek

Operations



KeyASIC Corporate Structures

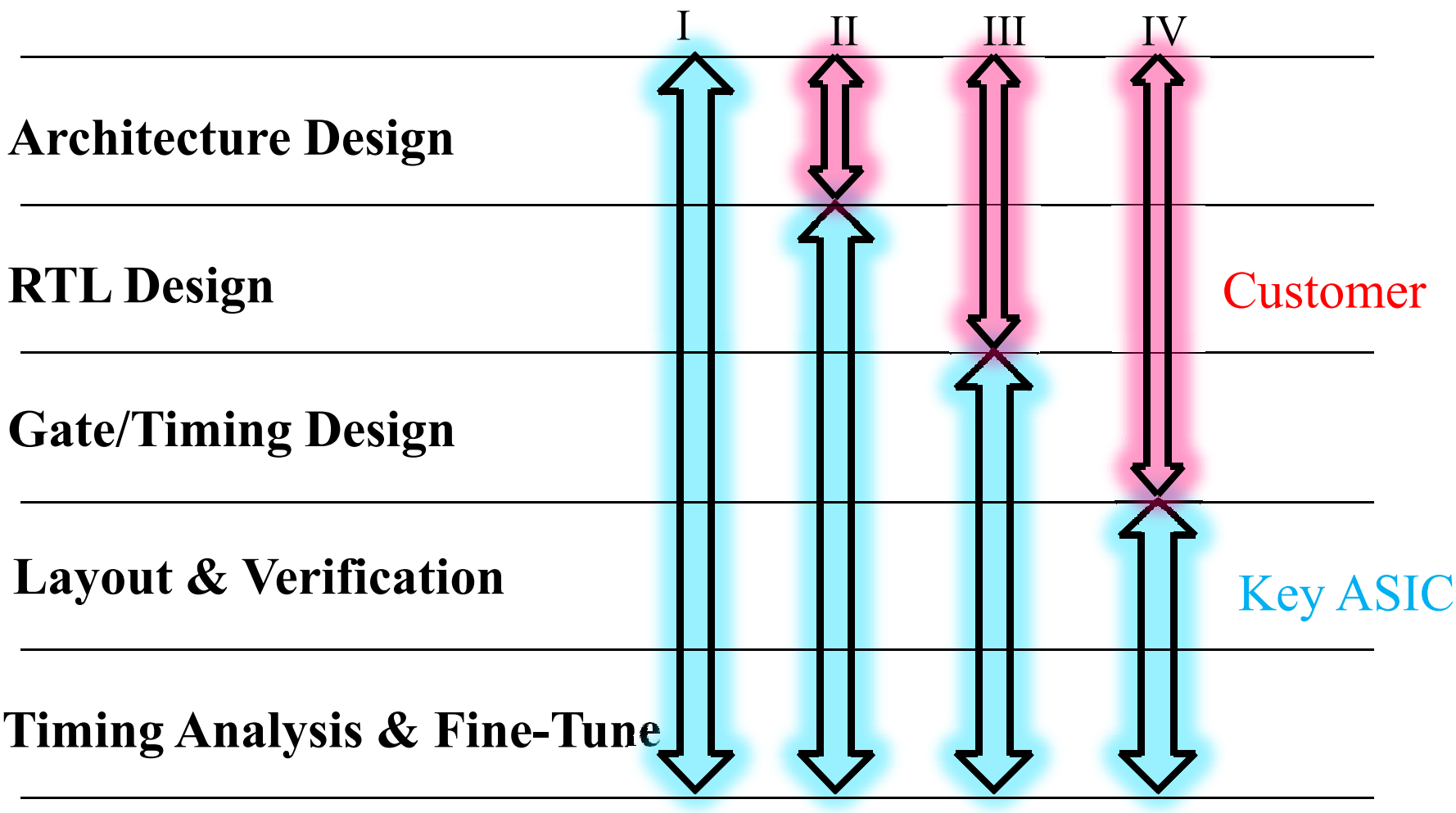


Technology Division

Engineering Division	Products	Customers
CSSP, ASIC ODM (Chip, System, OS, Drivers, Applications)	Wafers, chips, Systems board, SW	System ASIC Companies
ASIC/ SoC Implementation and Optimization (Design Methodology, Tools development, Platform, etc)	Wafer, Chips, NRE, Platforms	System ASIC/ Fabless Design Companies
Design and Foundry Enablement PDK, Std Cells, Memory, I/O, Analog IP, CPU, USB, etc.	IP, PDK, Design Flow, Calibrations	Foundries, Fabless Design Companies

ASIC DESIGN SERVICE

Flexible Service Offering



Design Service Models

	RTL to GDS Service	RTL to Wafer Service	RTL to Turnkey Service	Gate to GDS Service	Gate to Wafer Service	Gate to Turnkey Service
Library / IP Qualification	●	●	●	●	●	●
RTL QA Solution	●	●	●			
Timing Closure	●	●	●	●	●	●
DFT Solution	●	●	●	●	●	●
Power Solution	●	●	●	●	●	●
Reliability Solution	●	●	●	●	●	●
Physical Design Solution	●	●	●	●	●	●
Wafer / Fab. Solution		●	●		●	●
Assembly / Testing Solution			●			●

- RTL to GDS
- Netlist to GDS
- GDS to GDS
- Arch Implementation
- RTL Optimization
- Circuit Optimization
- Layout Optimization
- IP Implementation/Porting
- PDK development/Validation
- Turnkey service

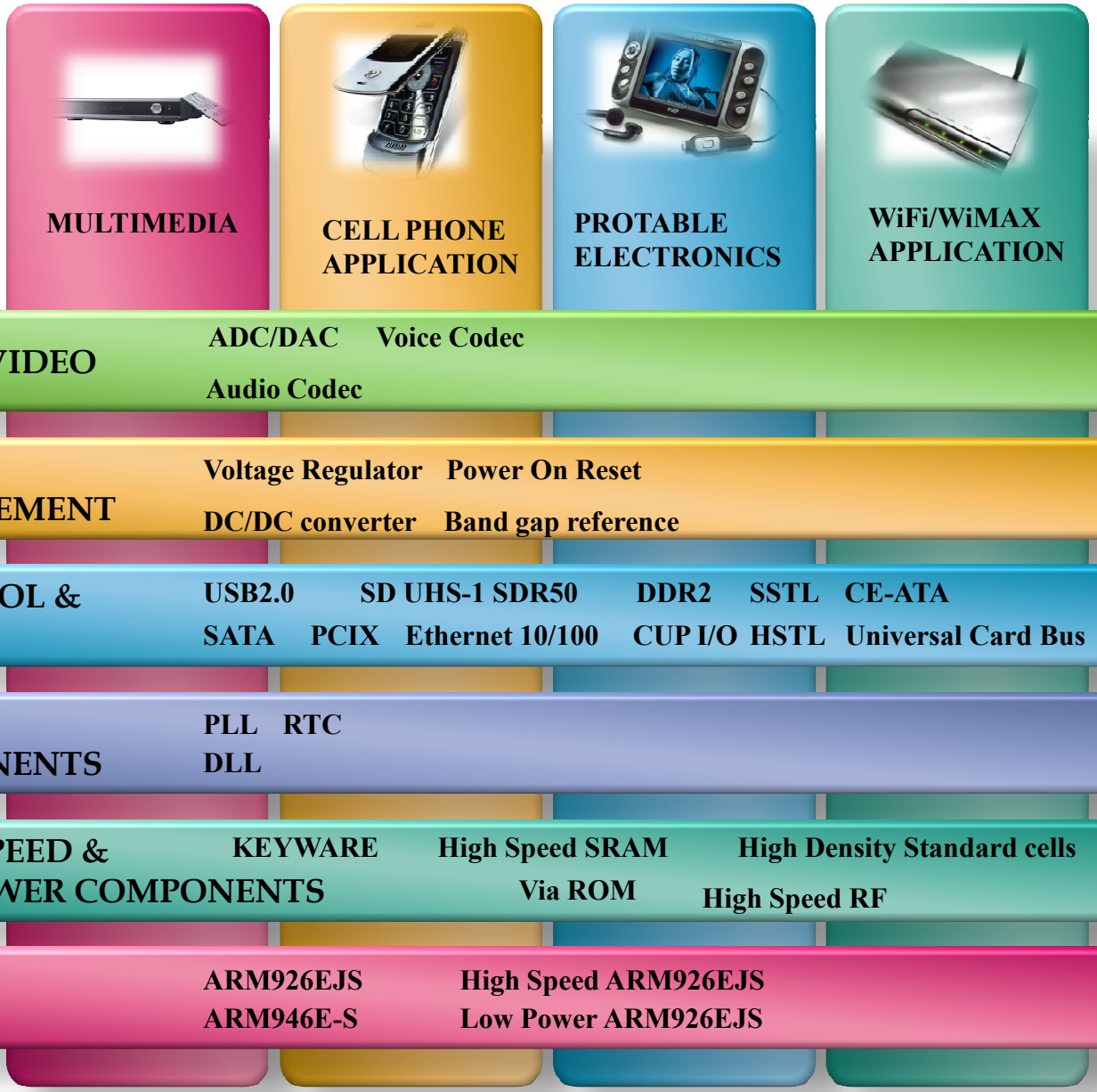
Design Env & EDA Tools

Design Flow & Function	cadence	SYNOPSYS	Mentor Graphics	
RTL Coverage	NC Verilog (Incisive 13.2)	VCS (2014.12-1)		
RTL Analysis		nLint (2013.09)		
Dynamic Sim	NC Verilog (Incisive 13.2)	VCS (2014.12-1)		
Logic Synthesis	RTL Compiler (RC14.2)	Design Compiler (2012.06-SP4)		
STA Signoff Tool	ETS (ETS11.11)	Prime-Time (SI) (2013.12-SP3)		
Floor Planner	SOC Encounter	ICC (Astro) (2014.09-SP3)		
AP&R Related	SOC Encounter(EDIS11.11S071_1)	ICC (Astro)) (2014.09-SP3)		
RC Extractor		Star RC-XT (2012.06-SP3-1)	XRC (V2011.4)	
SI, Delay Calculator	ETS (ETS11.1_s071.1)	Prime-Time (SI) (2013.12-SP3)		
Power Analysis	EPS (EPS13.19)	PTPX (2011.12-SP1) Prime-Rail (2011.12-SP1)		
Formal Verification	Conformal (V12.10)	Formality (2014.09)		
DFT/MBIST/BSD		DFT Compiler (2012.06-SP4) BSD (2012.06-SP4)	Memory (2009.01) Architecture	
Layout Editor	Virtuoso-XL (5.1041-USR6.127.29)	Laker (2012.12-P1)		
Low Power Solution	Conformal-Low Power (v14.20.220)			
DRC/ERC/LVS Signoff			Calibre (V2010.1)	
Misllaneous	Composer(IC5.1041)	Hspice(2014.09-SP1)		

Available FAB Process

	0.35u	0.18u	0.16u	0.13u	0.11u	90nm	65nm	55nm	40nm
Fujitsu						X	X	X	
Global Foundries		X		X			X	X	X
Silterra		X	X	X	X				
SMIC		X(eFlash)	X	X	X		X	X	
TSMC		RF & SiGe BiCMOS							
MXIC	X								
UMC		X(eFlash)		X			X	X	X
CSMC		X		X					
HHGrace		X		X(eFlash)					

IP Focus


MULTIMEDIA
CELL PHONE APPLICATION
PROTABLE ELECTRONICS
WiFi/WiMAX APPLICATION
AUDIO/VIDEO
ADC/DAC Voice Codec
Audio Codec
POWER MANAGEMENT
Voltage Regulator Power On Reset
DC/DC converter Band gap reference
PROTOCOL & I/O
USB2.0 SD UHS-1 SDR50 DDR2 SSTL CE-ATA
SATA PCIX Ethernet 10/100 CUP I/O HSTL Universal Card Bus
CLOCKS COMPONENTS
PLL RTC
DLL
HIGH SPEED & LOW POWER COMPONENTS
KEYWARE High Speed SRAM High Density Standard cells
Via ROM High Speed RF
CPUs
ARM926EJS High Speed ARM926EJS
ARM946E-S Low Power ARM926EJS

One-Stop Solution Production Management

Product Engineering (NPI)
Develop DFM/DFT/test plan specification
Manage product qualification project
Perform product characterization
Transfer design to wafer fabrication foundry
Manage product definition for system /BOM
Address customer issues
Manage product yield /quality and cost

Test Engineering / QA
Manage test H/W & S/W project
Transfer product to test site
Dispose suspected material in test
Implement long term QA program
Manage document control
Address customer issues

Testing Development Activity
Test hardware / software development
Manage reliability in board fabrication
Manage reliability test activities

Production Planning /Control
Manage manufacturing planning system
Implement capacity planning process
Forecast/ build plan /pack out/ ship
Manage backlog
Track and control inventory

Packaging Engineering
Manage design rules
Design & develop packaging
- Package outline design, substrate design
- Bonding diagram and BOM

Define package/ marking /packing specification
Improve package ,yield, cost and reliability
Dispose suspected materials in assembly

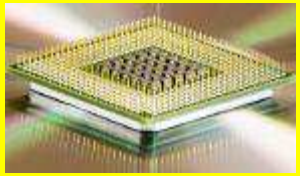
Overall Production Activity
Wafer fabrication
Assembly operation
Test / visual/ packing/ shipping operations

ASSP

ASSP System, Chip and Software Design and Production

Applications

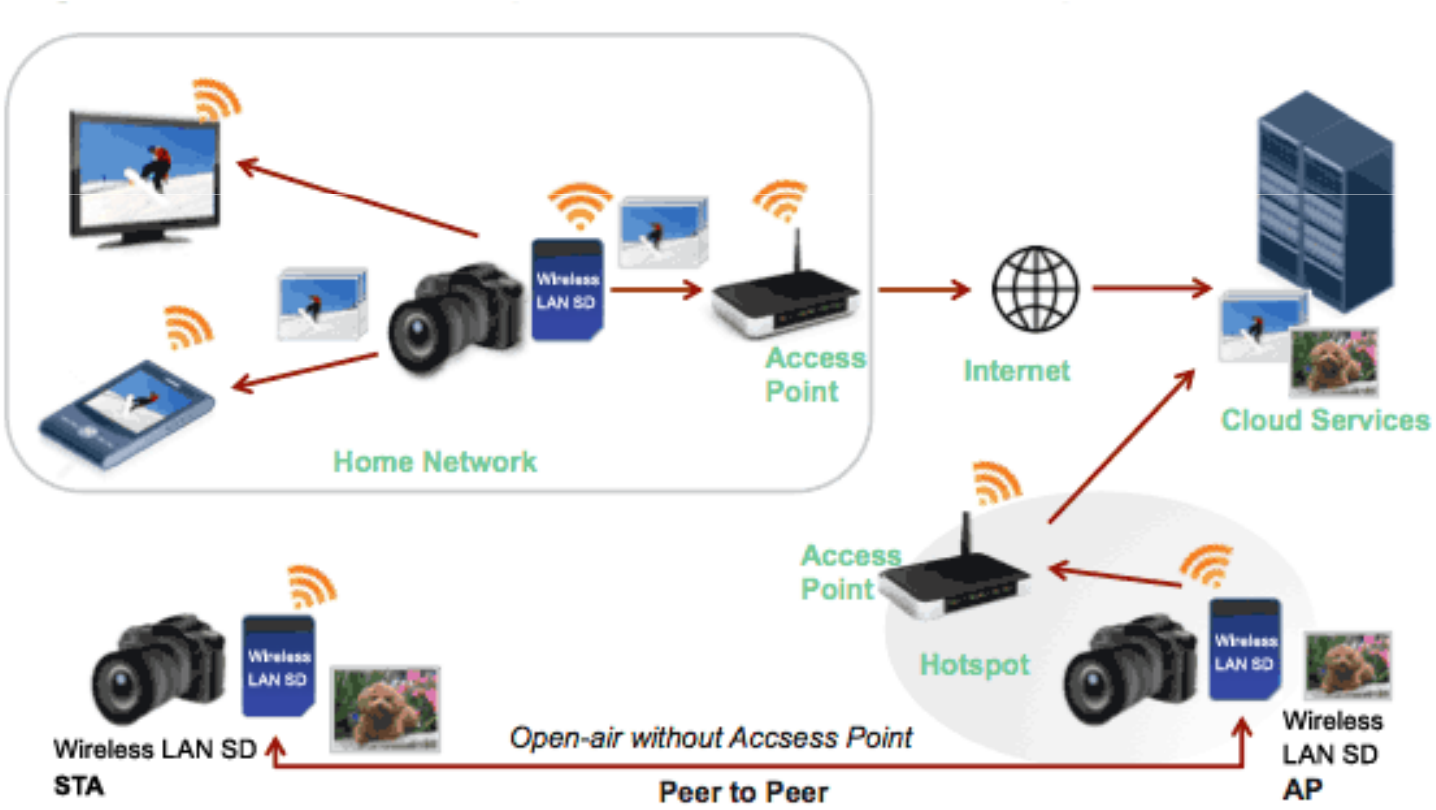
OS
(Drivers)



KA SOC ASSP Application Roadmap (I)

WiFi SDXC/3.0 Card

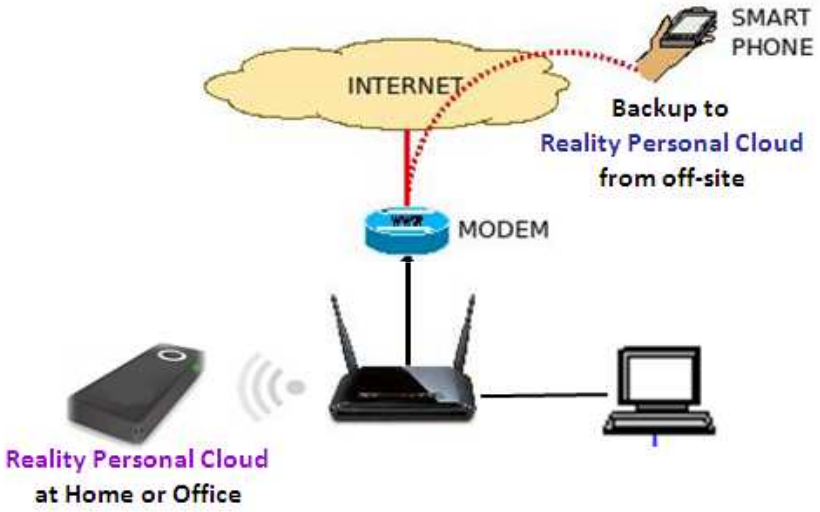
- Instant share and backup photo, video and audio files via wireless network ; **NO More PC**



KA SOC ASSP Application Roadmap (II)

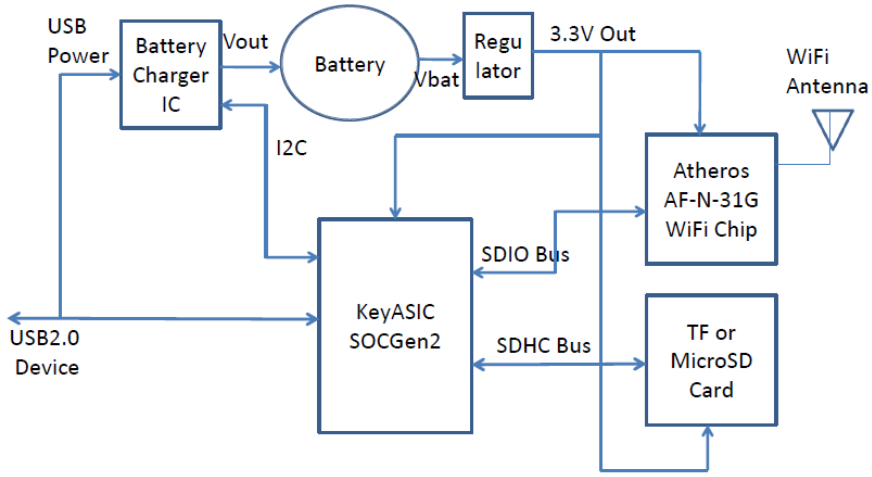
WiFi FD 3.0 Drive

- Behave as a Mobile Cloud for Smart Phone & Tablet



User Scenario

WiFI FD Drive Functional Block Diagram



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